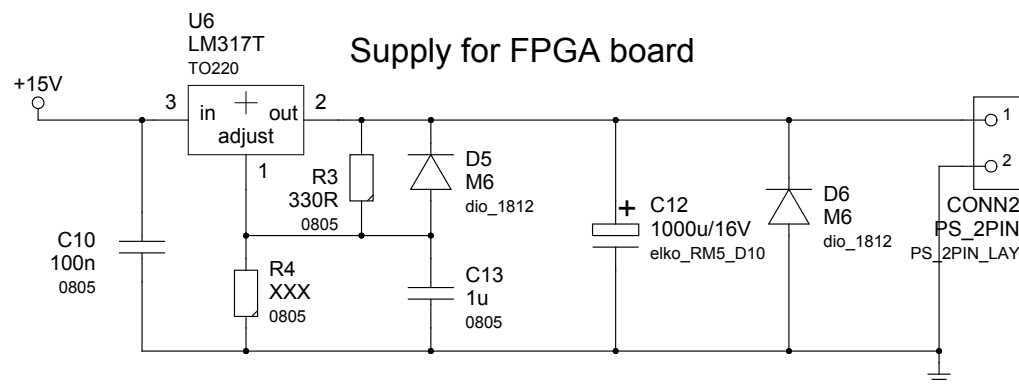
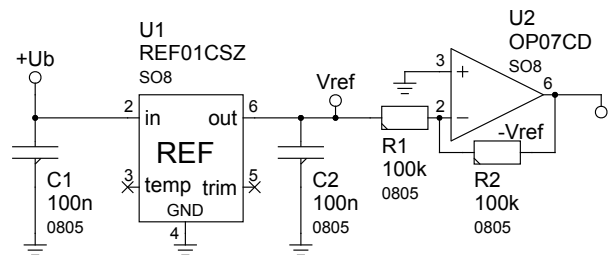
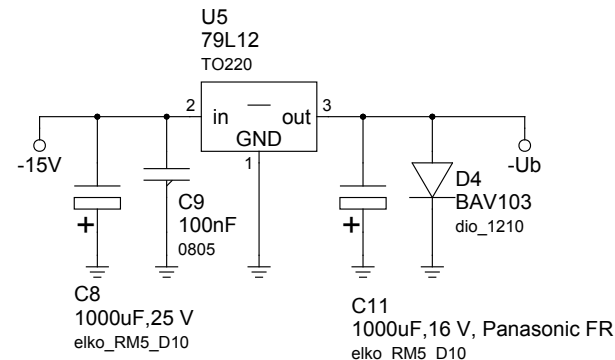
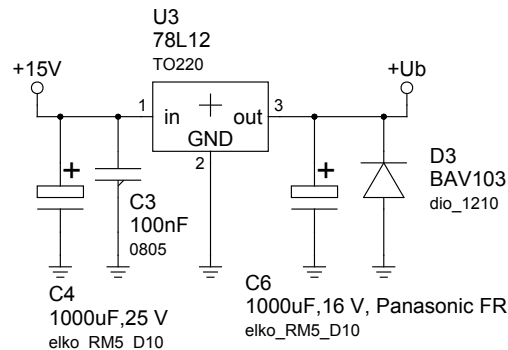
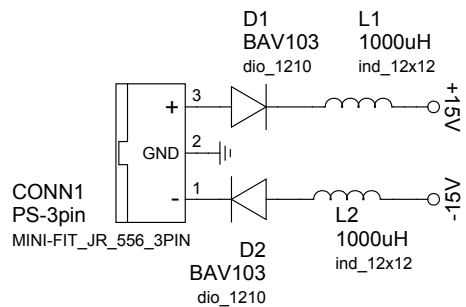


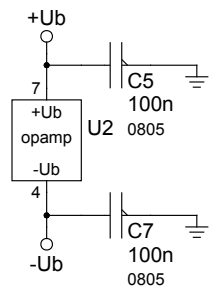
connection

TITLE: <b>Overview</b>		REV.: <b>3.0</b>
		DATE: <b>24.08.2017</b>
PROJECT: <b>ioboard</b>		DRAWN BY: <b>H. Albers</b>
FILE: <b>ioboard.sch</b>	PAGE: <b>1/7</b>	

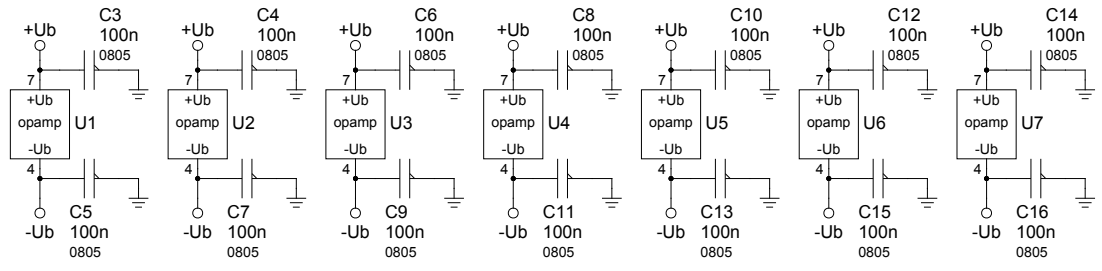
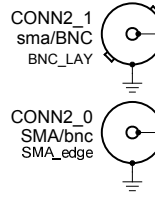
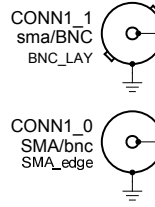
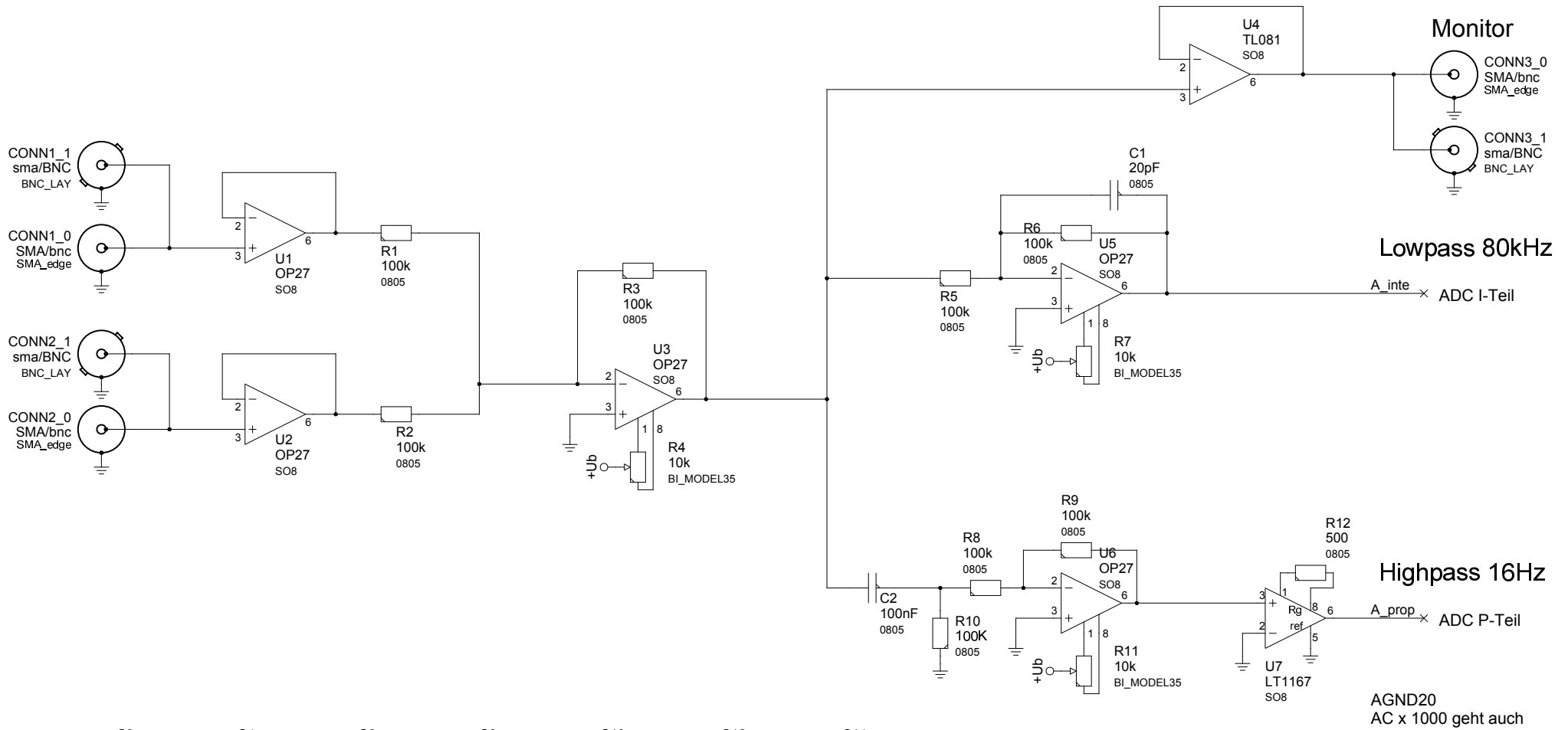


xxx = 1kR for 5V  
xxx = 1.8kR for 8V

$$U_{out} = 1.25V * (1 + R1/R2) + 50uA * R1$$



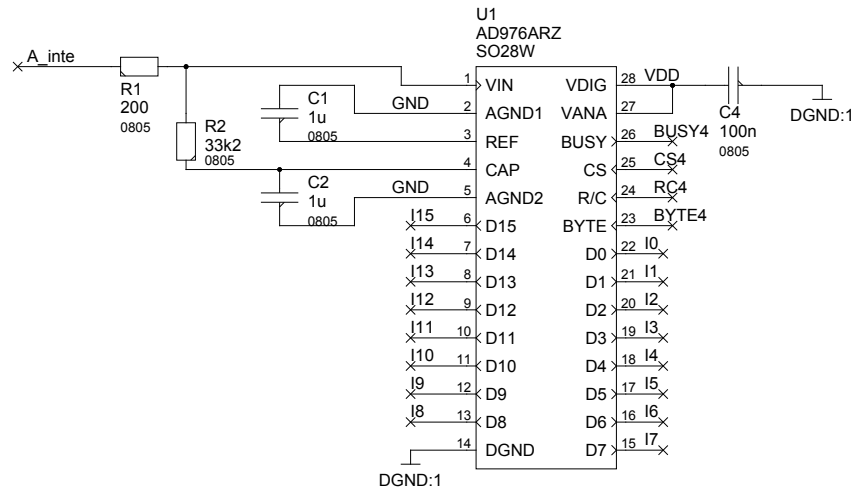
TITLE: PROJECT:		Supply Project		1.0
				REV.:
Supply.sch FILE:		H. Albers DRAWN BY:		25.08.2017
				DATE:
				PAGE: 2/7



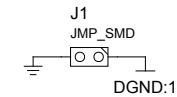
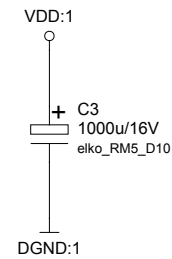
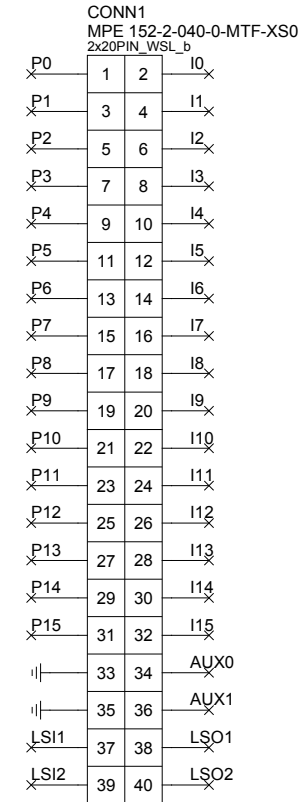
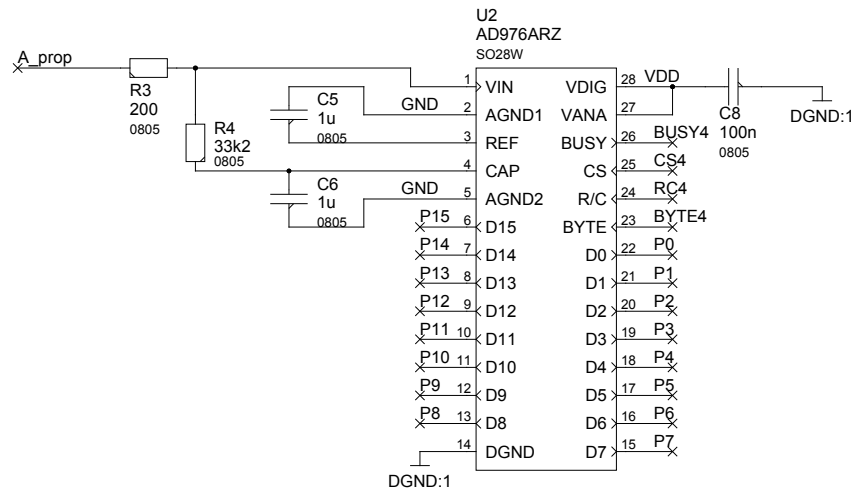
XXX nur bestücken, wenn Verstärkung größer 1 ist

<b>Input</b>		<b>3.0</b>
TITLE:	REV.:	
PROJECT:	loboard	25.08.2017
FILE:	input.sch	DATE:
	H. Albers	PAGE: 3 / 7
	DRAWN BY:	

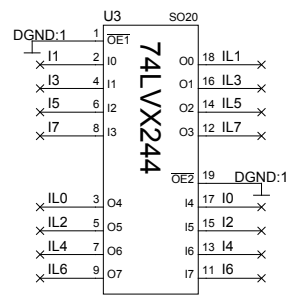
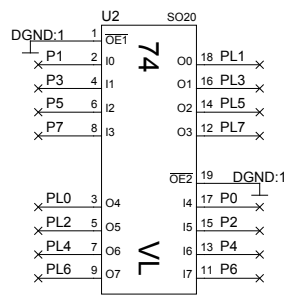
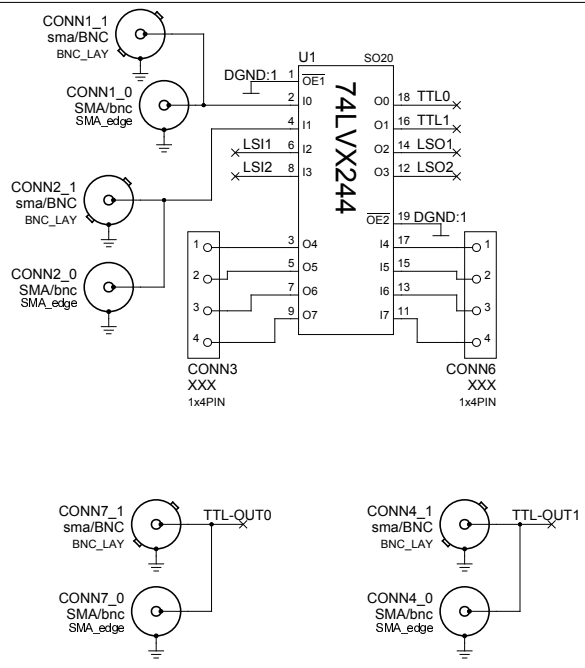
## AD-Converter I-Part



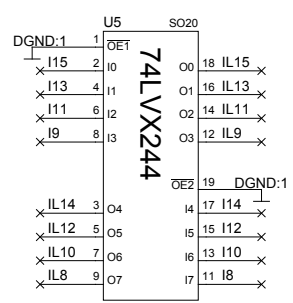
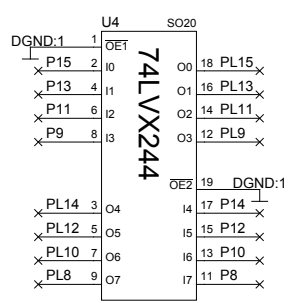
## AD-Converter P-Part



TITLE: <b>AD-Converter</b>		REV.: 1.0
		PROJECT: AD-Converter
FILE: filename.sch H. Albers		DATE: 24.08.2017
DRAWN BY:		PAGE: 4/7

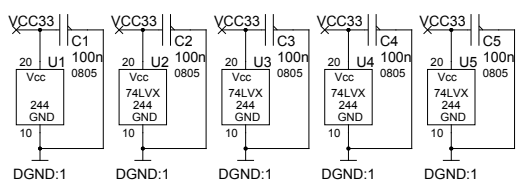
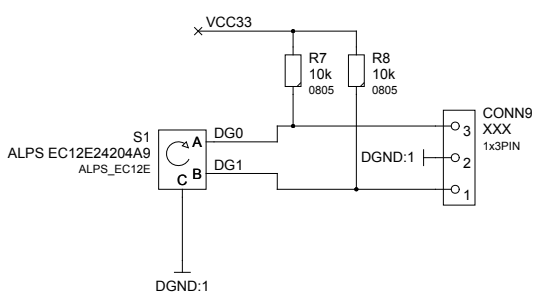


X244



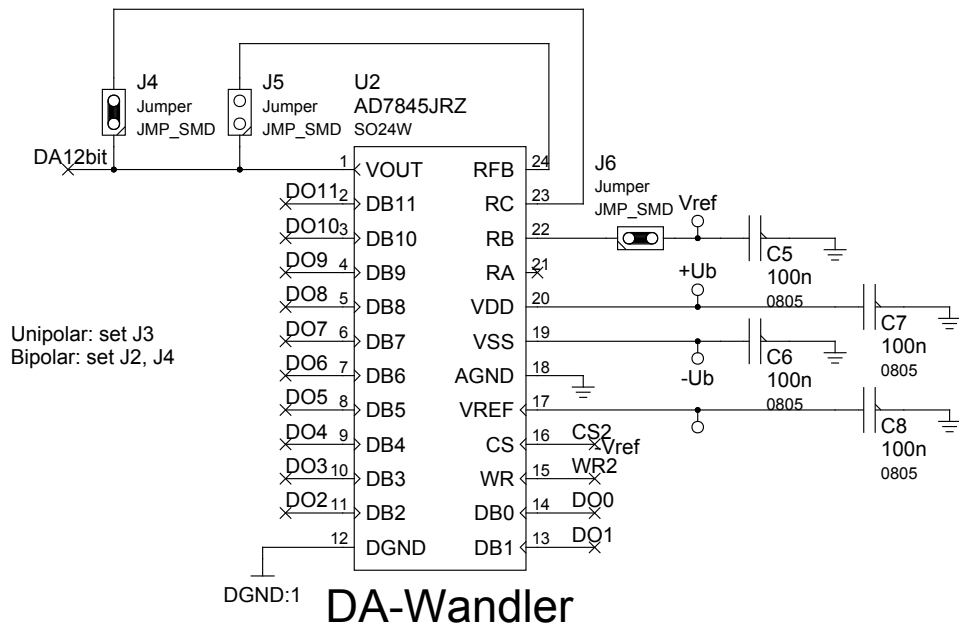
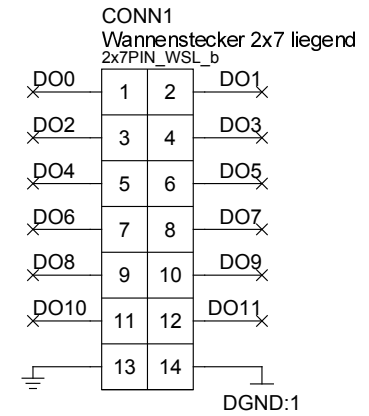
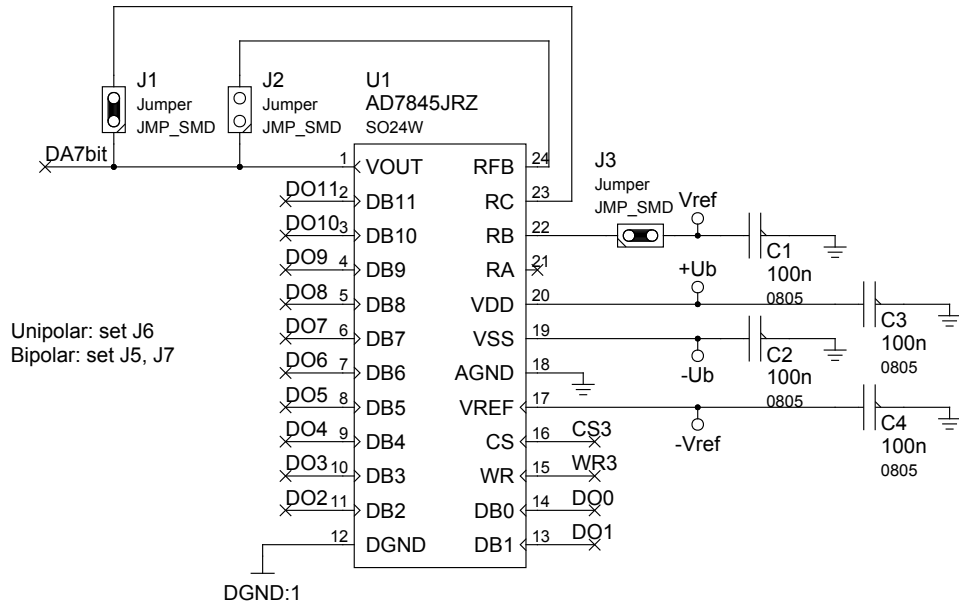
GPIO 0		CONN10 Wannenstecker 40-Pol 2x20PIN_WSL_b	
X1	IO1	2	X
X4	IO2	4	TTL1
X5	IO3	6	TTL-OUT0
X7	IO4	8	TTL-OUT1
X9	IO6	10	AUX0
X11	IO8	12	X
X12	VCC5	GND	X
X13	IO10	14	X
X15	IO12	16	X
X17	IO14	18	X
X19	IO16	20	DG0
X21	IO18	22	DG1
X23	IO20	24	PL1
X25	IO22	26	PL3
X27	IO24	28	PL5
X29	VCC33	GND	X
X31	IO26	32	PL7
X33	IO28	34	PL9
X35	IO30	36	PL11
X37	IO32	38	PL13
X39	IO34	40	PL15

GPIO 1		CONN11 Wannenstecker 40-Pol 2x20PIN_WSL_b	
XCS2	IO0	2	WR2
XCS3	IO2	4	WR3
XDO0	IO4	6	DO1
XDO2	IO6	8	DO3
XDO4	IO8	10	DO5
XVDD	VCC5	GND	X
XDO6	IO10	12	DO7
XDO8	IO12	14	DO9
XDO10	IO14	16	DO11
XDO12	IO16	18	DO13
XDO14	IO18	20	DO15
XBUSY4	IO20	22	CS4
XRC4	IO22	24	BYTE4
XIL0	IO24	26	IL1
XIL2	IO26	28	IL3
XIL4	IO28	30	IL5
XVCC33	VCC33	GND	X
XIL6	IO30	32	IL7
XIL8	IO32	34	IL9
XIL10	IO34	36	IL11
XIL12	IO36	38	IL13
XIL14	IO38	40	IL15



<b>FPGA connection</b>		1.0
TITLE:	Project	REV.:
PROJECT:	FPGA-com.sch	24.08.2017
FILE:	H. Albers	DATE:
DRAWN BY:		PAGE: 5/7

# DA-Wandler

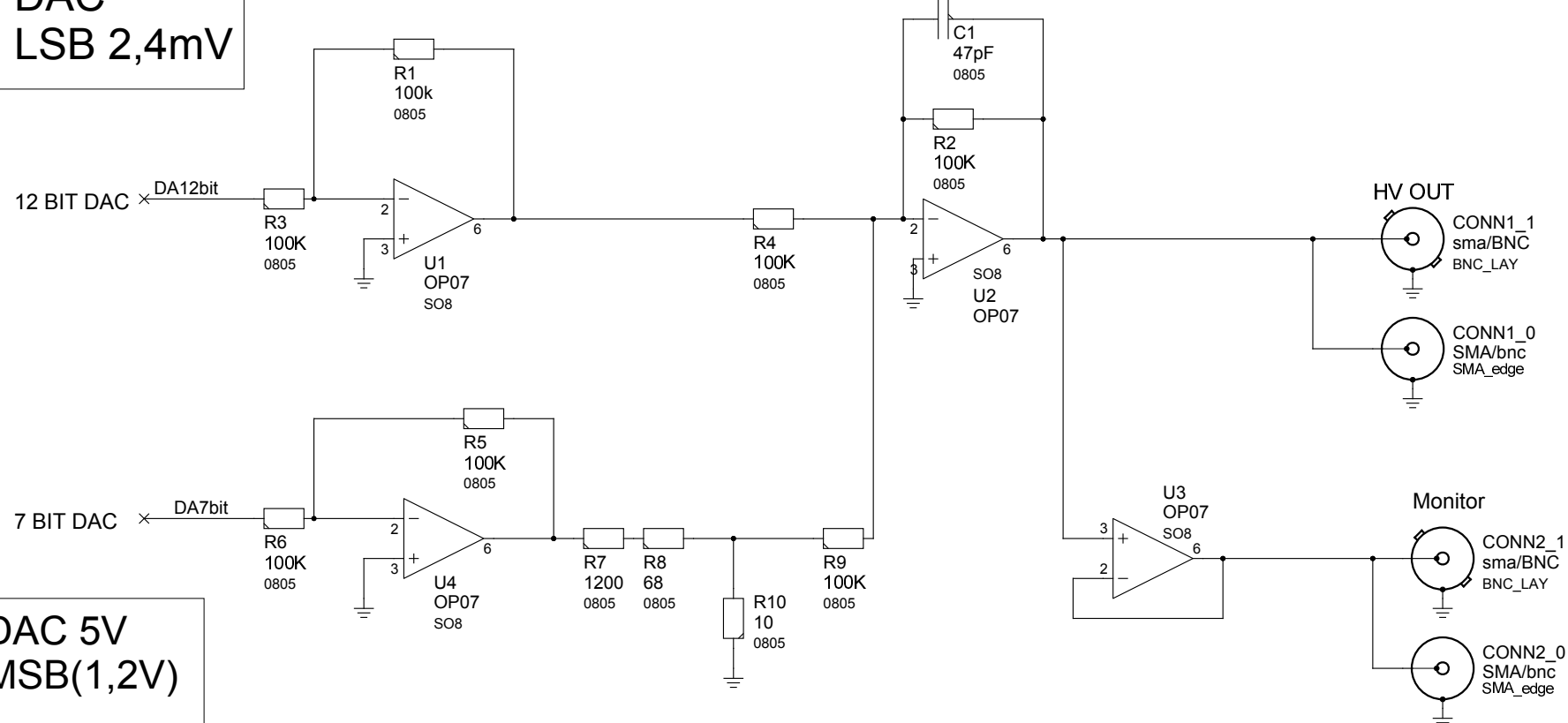


# DA-Wandler

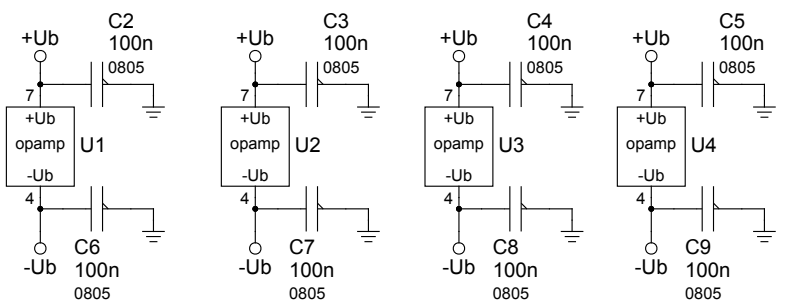
TITLE: <b>DA Converter</b>		REV.: <b>1.0</b>
PROJECT: <b>ioboard</b>		DATE: <b>24.08.2017</b>
DA_Converter.sch	H. Albers	DRAWN BY:
FILE:—		PAGE: <b>6/7</b>

DAC  
LSB 2,4mV

### Tiefpass 34kHz



DAC 5V  
MSB(1,2V)



"SMA/BNC" = SMA, Randbuchse  
oder BNC Einbaubuchse, liegend  
z.B. Amphenol B6252H5NPP3G50PBF

<h1>Output</h1>		<b>3.0</b>
TITLE:	REVISION:	
PROJECT:	25.08.2017	
FILE:	Output.sch	DATE:
	H. Albers	PAGE: 7/7
	DRAWN BY:	