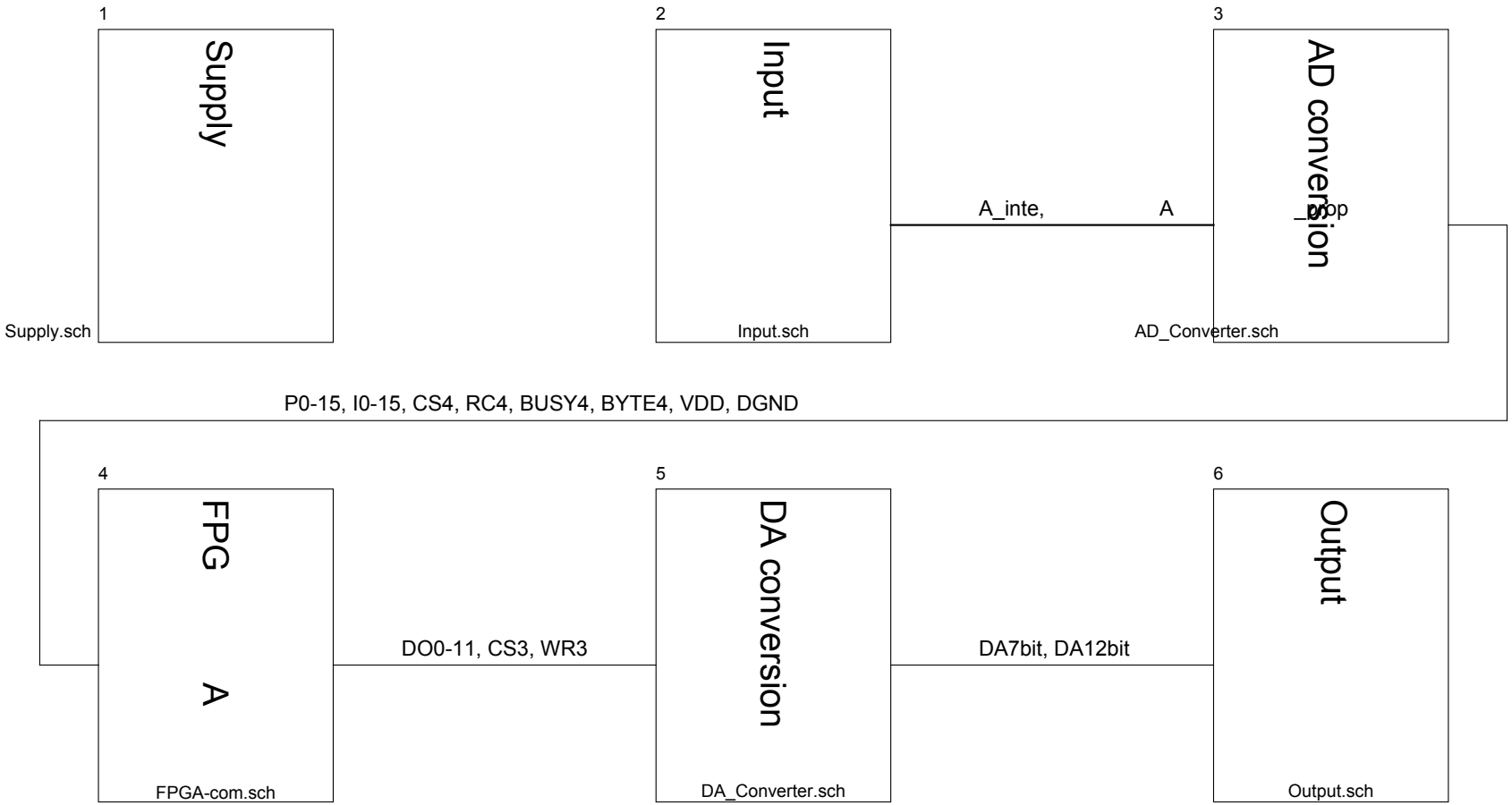
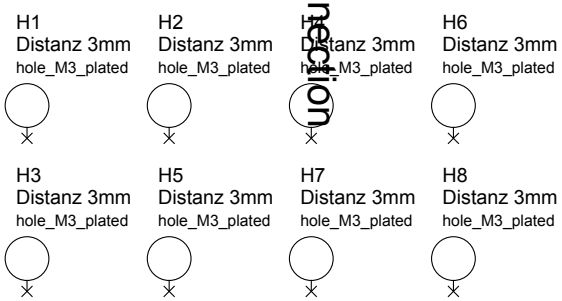
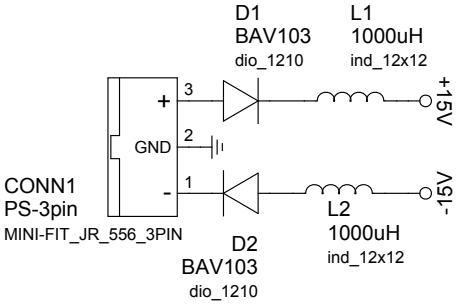
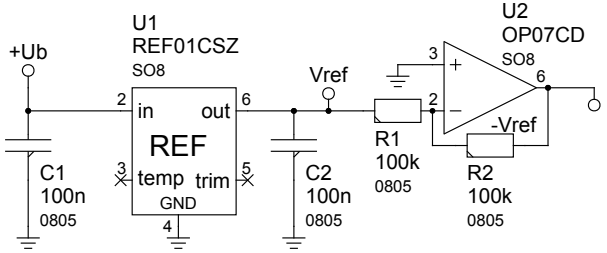
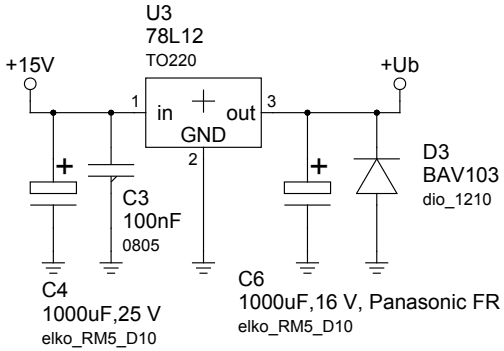


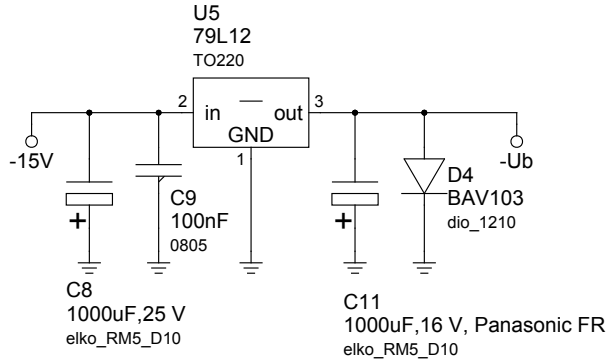


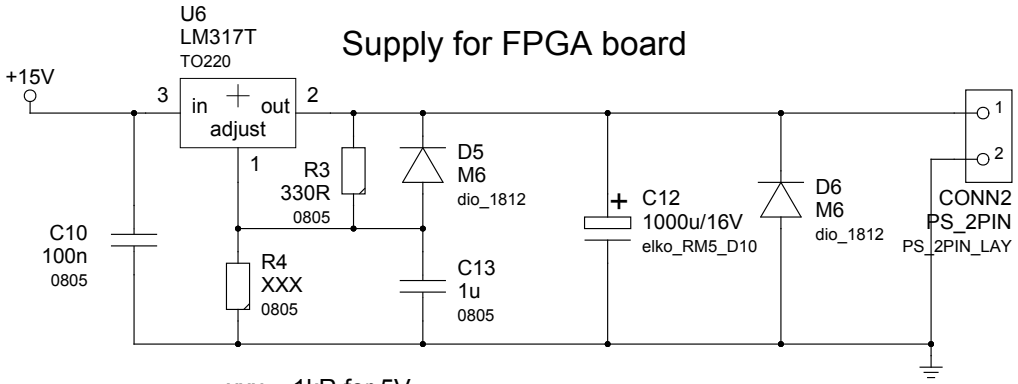
TITLE:	Overview	3.0 REV.:
PROJECT:	ioboard	24.08.2017 DATE:
FILE: ioboard.sch	DRAWN BY: H. Albers	PAGE: 1/7





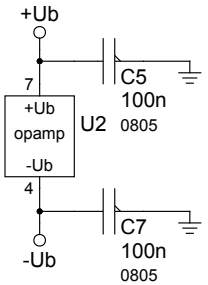




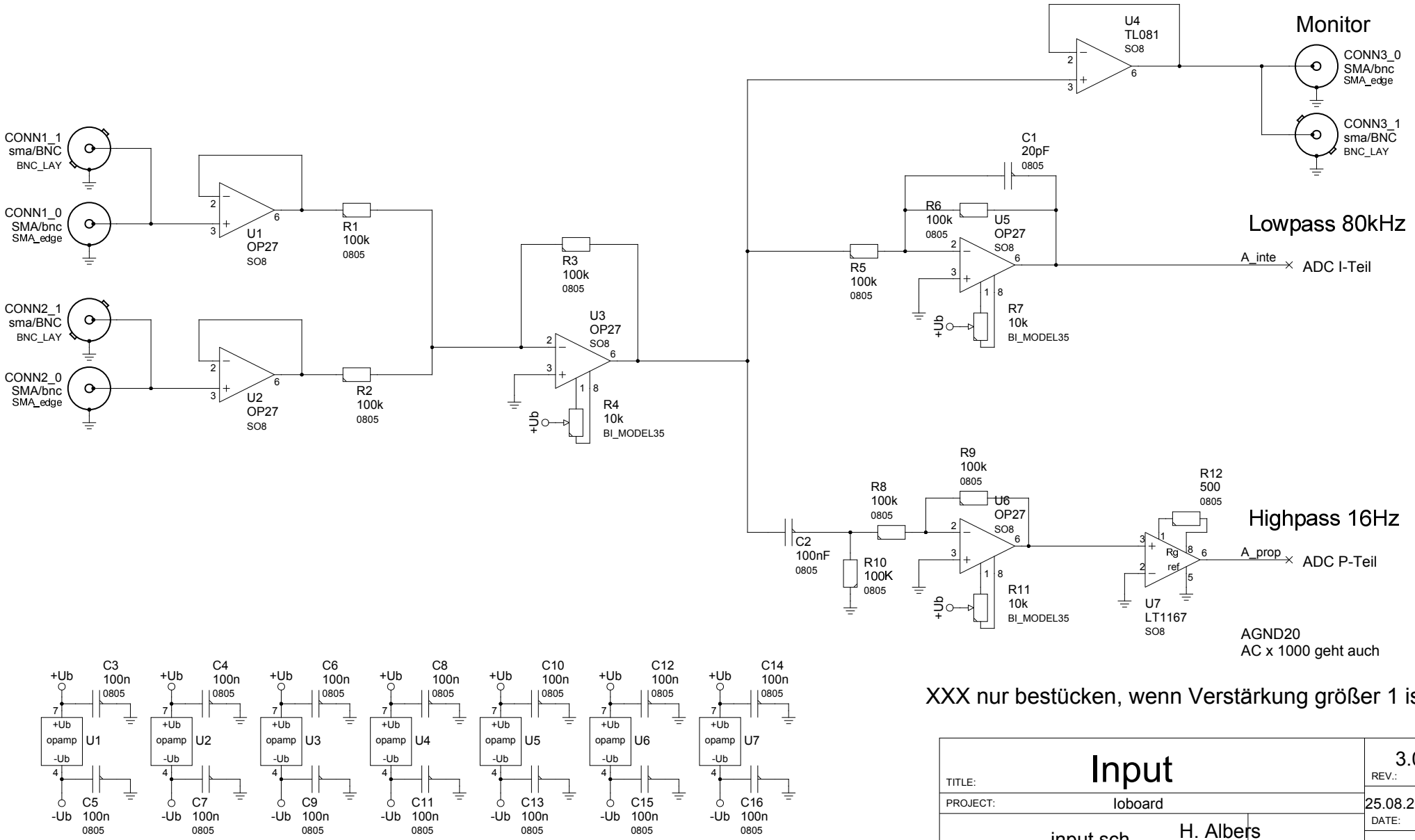


xxx = 1kR for 5V
xxx = 1.8kR for 8V

U_out = 1.25V * (1 + R1/R2) + 50uA * R1



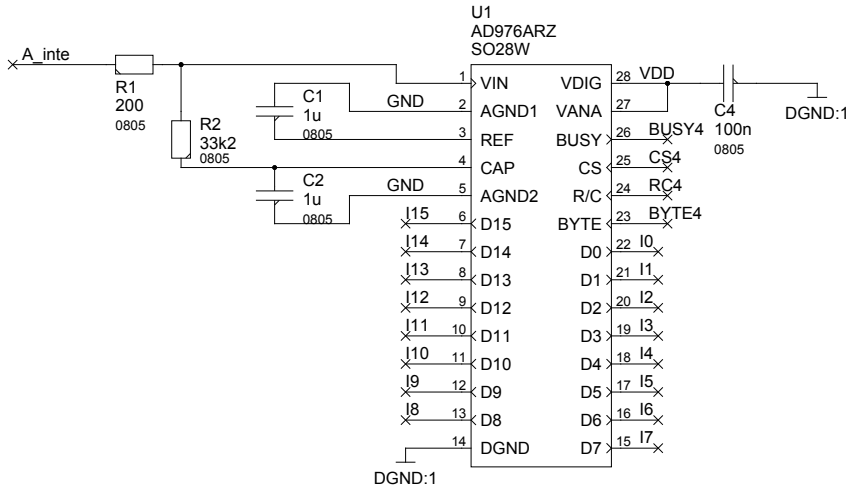
TITLE:	Supply	REV.: 1.0
PROJECT:	Project	DATE: 25.08.2017
FILE: Supply.sch	DRAWN BY: H. Albers	PAGE: 2/7



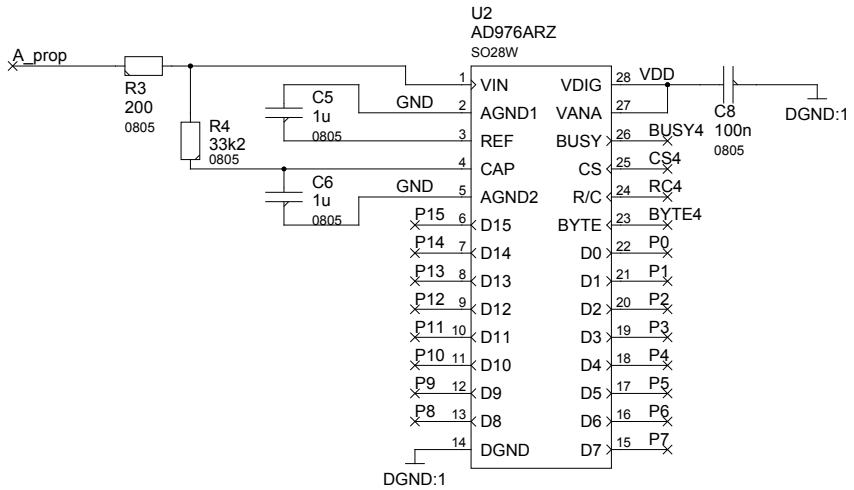
XXX nur bestücken, wenn Verstärkung größer 1 ist

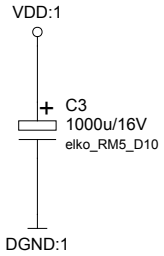
TITLE:	Input	REV.: 3.0
PROJECT:	loboard	DATE: 25.08.2017
FILE: input.sch	DRAWN BY: H. Albers	PAGE: 3 / 7

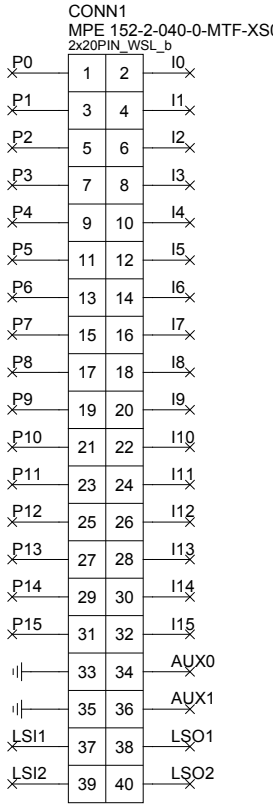
AD-Converter
I-Part

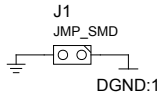


AD-Converter
P-Part

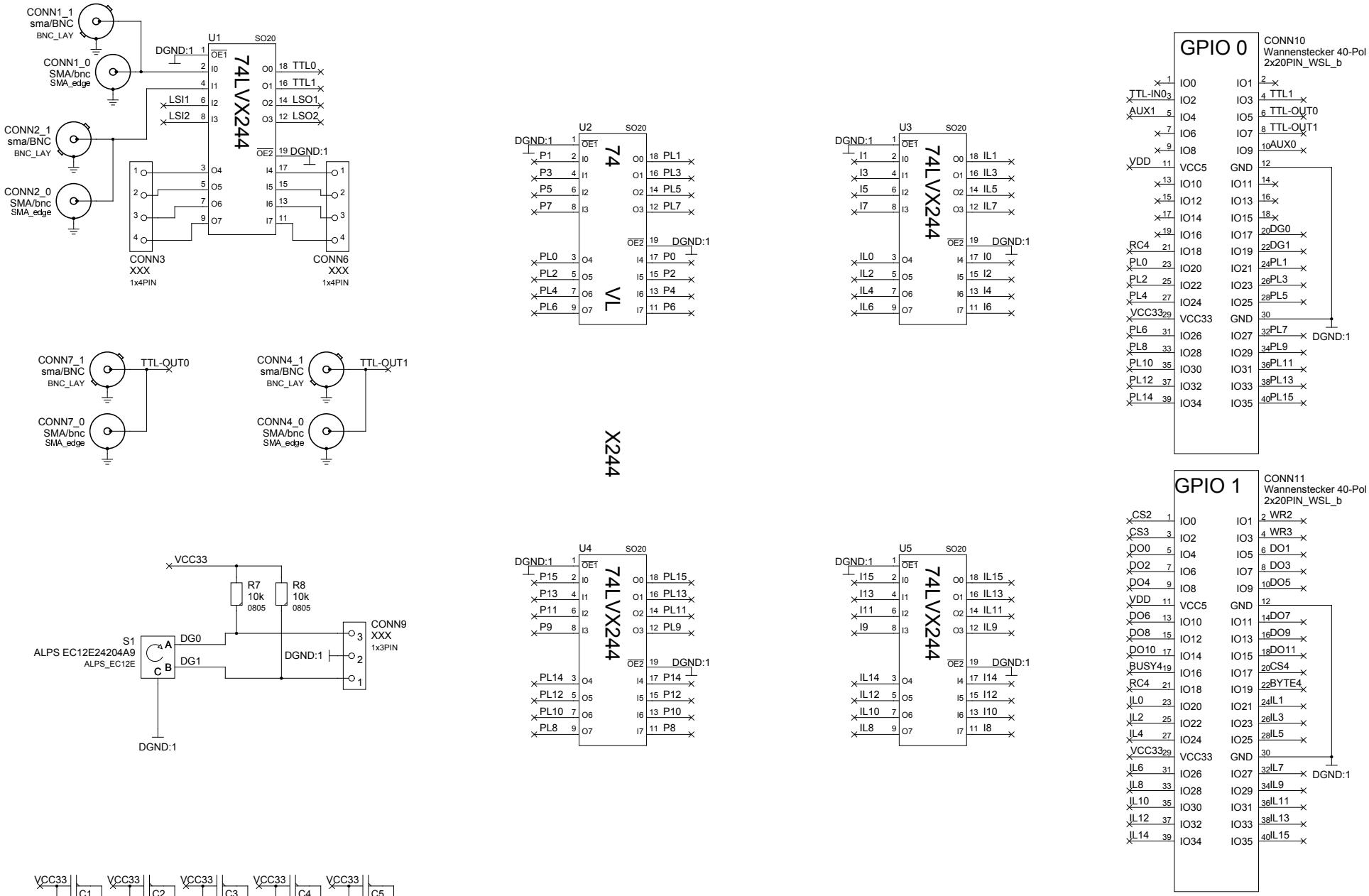








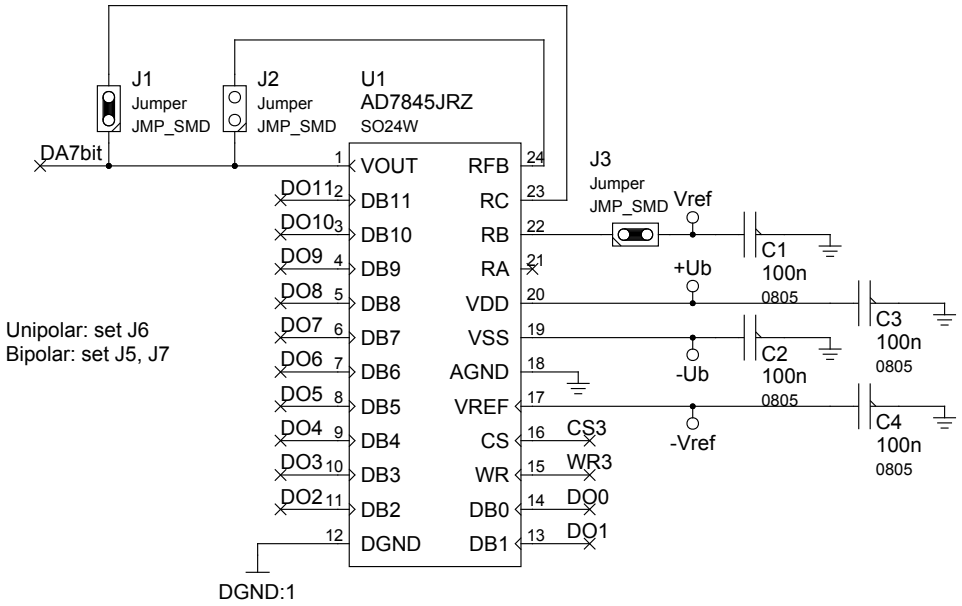
TITLE:	AD-Converter	REV.: 1.0
PROJECT:	AD-Converter	DATE: 24.08.2017
FILE: filename.sch	DRAWN BY: H. Albers	PAGE: 4/7

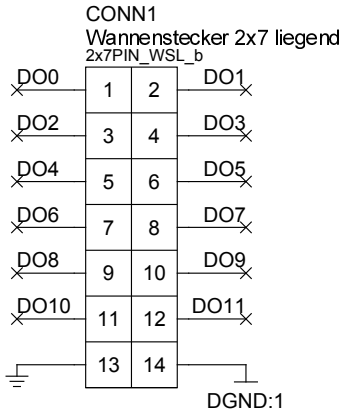


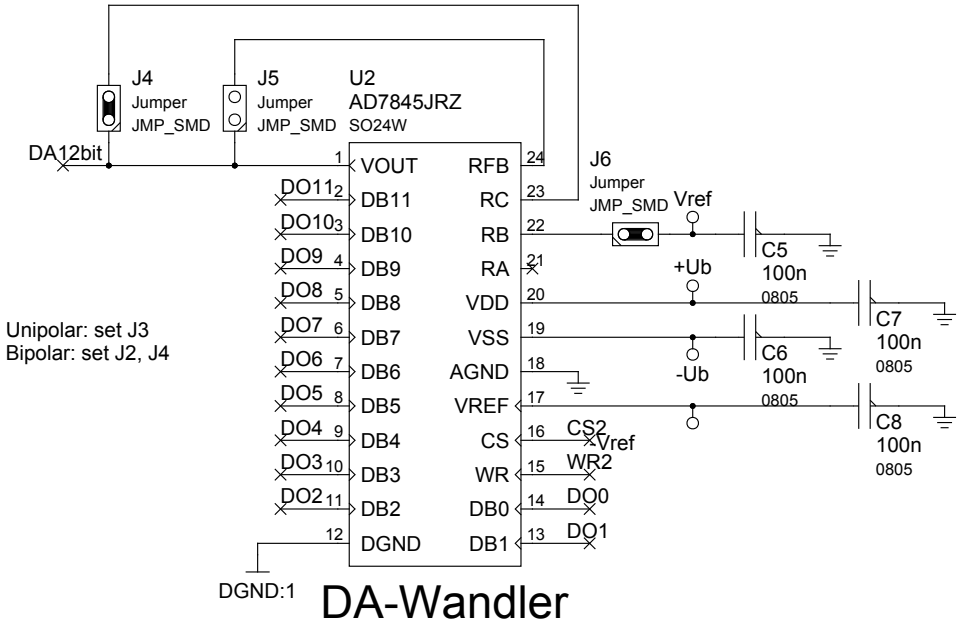
FPGA connection

TITLE:	FPGA connection
REV.:	1.0
PROJECT:	Project
DATE:	24.08.2017
FILE:	FPGA-com.sch
DRAWN BY:	H. Albers
PAGE:	5/7

DA-Wandler





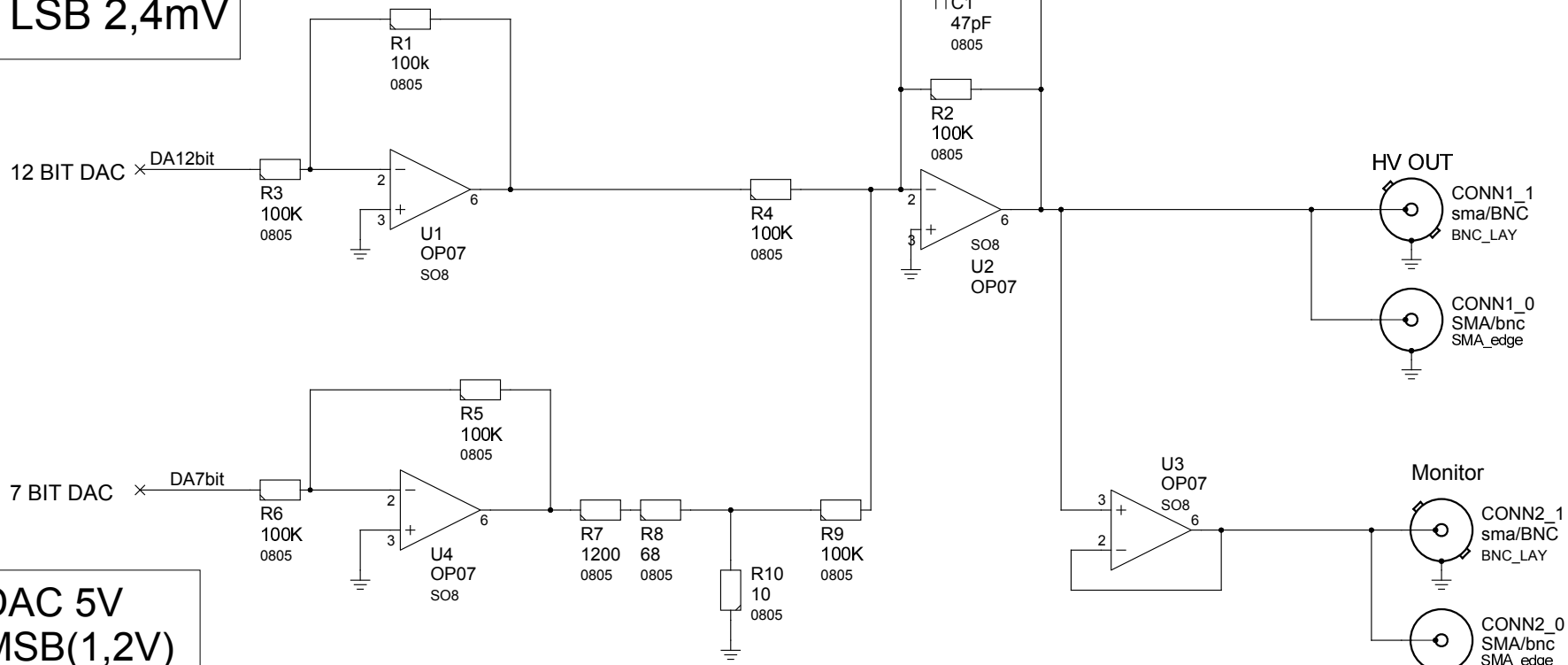


DA-Wandler

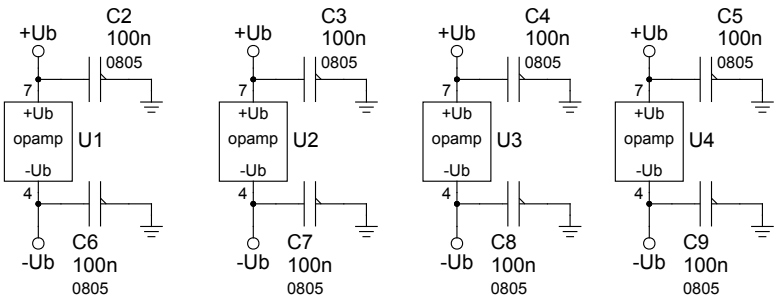
TITLE: DA Converter		REV.: 1.0
PROJECT: ioboard		DATE: 24.08.2017
FILE: DA_Converter.sch	DRAWN BY: H. Albers	PAGE: 6/7

Tiefpass 34kHz

DAC
LSB 2,4mV



DAC 5V
MSB(1,2V)



"SMA/BNC" = SMA, Randbuchse
oder BNC Einbaubuchse, liegend
z.B. Amphenol B6252H5NPP3G50PBF

TITLE:	Output	REV.: 3.0
PROJECT:	Ioboard	DATE: 25.08.2017
FILE: Output.sch	DRAWN BY: H. Albers	PAGE: 7/7